REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-27 are pending in the present application. Claims 1, 6, 11, 16, and 20 are amended by the present amendment.

In the outstanding Office Action, Claims 1-4, 6-9, 11-14, and 16-23 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,333,750 to Odryna et al. (hereinafter "Odryna"); Claims 5, 10, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Odryna in view of U.S. Patent No. 6,157,415 to Glen; and Claims 24-27 were rejected under 35 U.S.C. § 103(a) as unpatentable over Odryna.

Addressing now the rejection of Claims 1-4, 6-9, 11-14, and 16-23, as anticipated by Odryna, that rejection is respectfully traversed.

Amended Claim 1 is directed to an overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2. The overlay image processing device includes:

> a plurality of digital decoders configured to digitally decode a plurality of image signals;
>
> an image selector configured to directly receive outputs from each of the plurality of digital decoders and configured to select from among the plurality of digitally decoded image signals one (1) reference image signal and (n-1) number of superimposing image signals;
>
> a plurality of resolution converters configured to ~~receive respective outputs~~ directly receive the selected image signals output from the image selector, such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective desired resolutions, and to output the converted image signals to an image synthesizer,

> wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal. (shown in marked-up form)[1]

Thus, as recited, the claimed image selector is configured to (1) directly receive the outputs of a plurality of digital decoders, (2) select the reference image signal and superimposing signals from the plurality of digital decoder outputs, and (3) transmit the selected signals directly to the plurality of resolution converters. As recited, these limitations pertain to a single image selector. Independent Claims 1, 6, 11, 16, and 20 recite similar limitations.

In a non-limiting example, Figure 2 illustrates an embodiment of the claimed invention. As shown, a single image selector 116 directly receives outputs from each of three digital decoders 110, 112, 114, selects a reference image signal SD10 and superimposing signal SD20 from the outputs VPC(D), VS1(D), VS2(D) of the three digital decoders 110, 112, 114, and transmits the selected signals SD10, SD20 directly to two resolution converters 118, 120.[2]

The outstanding Office Action asserts that Figure 17 of Odryna teaches the claimed overlay image processing device. More particularly, the Office Action asserts that the system card 110 teaches the claimed image selector; and that the input interface cards A, B (by incorporating the BIVIDEO overlay card 180 of Figure 21) teach the claimed digital decoders and claimed resolution converters.[3] However, even assuming that the system card 110 functions as an image selector (not admitted), and further assuming that the BIVIDEO overlay card 180 contains digital decoders and resolution converters (not admitted), Odryna does not teach those components as having the claimed configuration of the features of Claim 1. That deficiency is now explained with respect to limitations (1) through (3) discussed above.

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[1] For support, see Figure 2 of the present application.
[2] Specification, page 4, line 17 — page 5, line 20.
[3] Office Action, 2/26/2004, pages 2-3.

With respect to the first (1) limitation, the input and output arrows of Figures 17 of Odryna show that the input interface cards A, B have outputs only to the pixel and control buses, and further show that the pixel and control buses do not have output to the system card 110. Therefore, as the system card 110 cannot receive (directly or indirectly) the outputs of the input interface cards A, B, those cards 110, A, B cannot teach the claimed configuration of the image selector and digital decoders of Claim 1.

With respect to the second (2) limitation, as the system card 110 cannot receive outputs from the interface input cards A, B, the system card 110 also cannot select image signals output from those cards A, B. Thus, even assuming the input interface cards A, B (by incorporating the BIVIDEO overlay card 180) contain digital decoders (not admitted), the system card 110 could not select image signals output from such digital decoders.

Furthermore, though the system card 110 is stated as "capable of receiving" data for use as a reference image,[4] there is no indication that the system card 110 selects a reference image signal. Moreover, there is no indication that the system card 110 selects both a reference image signal and a superimposing signal.

With respect to the third (3) limitation, Applicants note that input interface cards A, B cannot receive inputs, directly or indirectly, from the system card 110. Thus, even assuming that the input cards A, B (by incorporating the BIVIDEO overlay card 180) contain resolution converters (not admitted), such resolution converters could not receive selected image signals output from the system card 110. Further, even assuming the scaler 184 of the BIVIDEO overlay card 180 performs resolution conversion (not admitted),[5] the scaler 184 could not receive signals directly output by an image selector to the BIVIDEO overlay card 180 because of the placement of the broadcast video decoder 182.

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[4] Odryna, col. 16, lines 18-21.
[5] See Office Action, 2/26/2004, page 3.

In sum, Odryna teaches a hub system in which several types of input interface cards (*i.e.*, system card 110, analog input card 140, computer overlay card 160, and BIVIDEO overlay card 180) are connected to the front end of the pixel and control buses. Because only their outputs are connected to the front end of the pixel and control buses, the input interface cards A, B, C cannot be serially connected to one another. Consequently, regardless of whether the system card 110 and BIVIDEO overlay cards 180 contain components similar to the claimed features of Claim 1 (not admitted), such components cannot teach the serial connections of the claimed features.

Accordingly, for the reasons stated above, Applicants respectfully request that the rejection of Claims 1-4, 6-9, 11-14, and 16-23 under § 102(e) as anticipated by Odryna, as well as the rejections of Claims 5, 10, 15, and 24-27 under § 103(a) as unpatentable over Odryna, be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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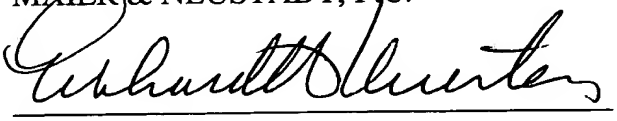

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